

STP80NF10FP

N-channel 100V - 0.012 Ω - 38A - TO-220FP Low gate charge STripFETTM II Power MOSFET

General features

Туре	V _{DSS}	R _{DS(on)}	I _D ⁽¹⁾
STP80NF10FP	100V	<0.015Ω	38A

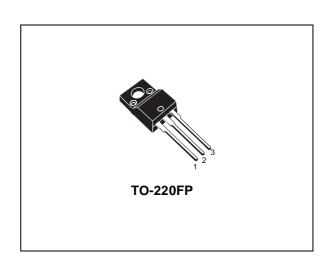
- Exceptional dv/dt capability
- 100% Avalanche tested
- Application oriented characterization

Description

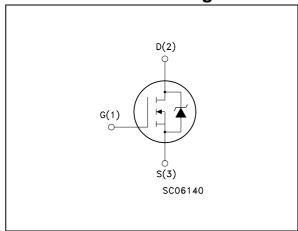
This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced highefficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

Applications

■ Switching application



Internal schematic diagram



Order codes

Part number	nber Marking Package		Packaging
STP80NF10FP	P80NF10FP	TO-220FP	Tube

Contents STP80NF10FP

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STP80NF10FP Electrical ratings

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} = 0)	100	V
V _{GS}	Gate- source voltage	±20	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25°C	38	Α
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100°C	27	Α
I _{DM} ⁽²⁾	Drain current (pulsed)	152	Α
P _{TOT}	Total dissipation at T _C = 25°C	45	W
	Derating factor	0.3	W/°C
dv/dt (3)	Peak diode recovery voltage slope	9	V/ns
E _{AS} ⁽⁴⁾	Single pulse avalanche energy	350	mJ
V _{ISO}	Insulation withstand voltage (DC)	2500	V
T _{stg} Tj	Storage temperature Operating junction temperature	-55 to 175	°C

^{1.} Limited by Package

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case Max	3.33	°C/W
Rthj-amb	Thermal resistance junction-ambient Max	62.5	°C/W
T _I	Maximum lead temperature for soldering purpose	300	°C

^{2.} Pulse width limited by safe operating area

^{3.} I_{SD} <80A, di/dt < 300A/ μ s, V_{DD} =80% $V_{(BR)DSS}$

^{4.} Starting Tj = 25°C, I_D = 80A, V_{DD} = 50V

Electrical characteristics STP80NF10FP

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test condictions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	100			٧
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating @125°C			1 10	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 40A		0.012	0.015	Ω

Table 4. Dynamic

Symbol	Parameter	Test condictions	Min.	Тур.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} =25V , I _D =40 A		80		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, $ $V_{GS} = 0$		4300 600 230		pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 80V, I_{D} = 80A,$ $V_{GS} = 10V$		140 23 51	189	nC nC nC

^{1.} Pulsed: pulse duration = 300 μ s, duty cycle 1.5 %

Table 5. Switching times

Symbol	Parameter	Test condictions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	\/ - 50\/ - 40 \		40		ns
t _r	Rise time	$V_{DD} = 50V, I_{D} = 40A,$ $R_{G} = 4.7\Omega, V_{GS} = 10V$		145		ns
t _{d(off)}	Turn-off-delay time	(see Figure 14)		134		ns
t _f	Fall time	(See Figure 14)		115		ns

Table 6. Source drain diode

Symbol	Parameter	Test condictions	Min	Тур.	Max	Unit
I _{SD}	Source-drain current				38	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				152	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 80A, V _{GS} = 0			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} =80A, V_{DD} = 50V di/dt = 100A/ μ s, T_j =150°C		155 850 11		ns nC A

^{1.} Pulse width limited by safe operating area

^{2.} Pulsed: pulse duration = 300 μ s, duty cycle 1.5 %

Electrical characteristics STP80NF10FP

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance

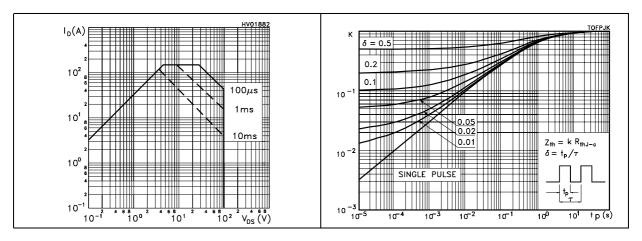


Figure 3. Output characterisics

Figure 4. Transfer characteristics

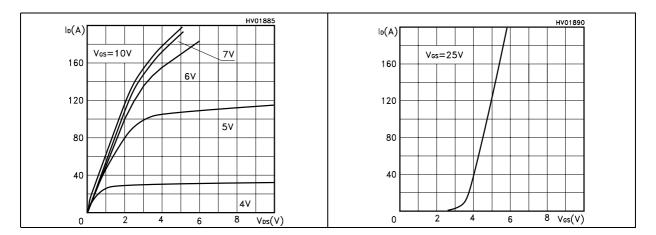
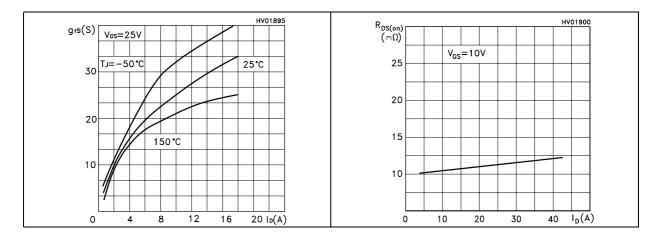


Figure 5. Transconductance

Figure 6. Static drain-source on resistance



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Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

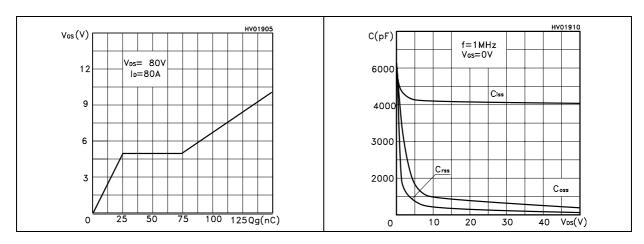


Figure 9. Normalized gate threshold voltage Figure 10. Normalized on resistance vs vs temperature temperature

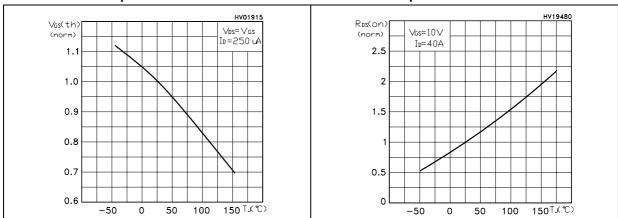
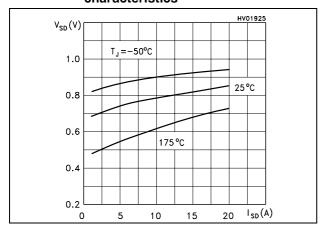


Figure 11. Source-drain diode forward characteristics



Test circuit STP80NF10FP

3 Test circuit

Figure 12. Switching times test circuit for resistive load

Figure 13. Gate charge test circuit

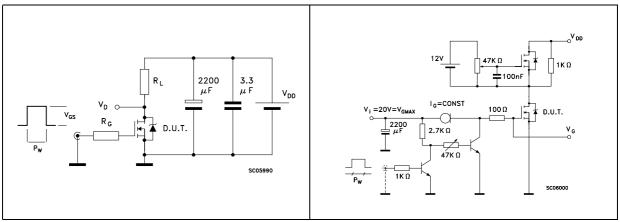


Figure 14. Test circuit for inductive load switching and diode recovery times

Figure 15. Unclamped inductive load test circuit

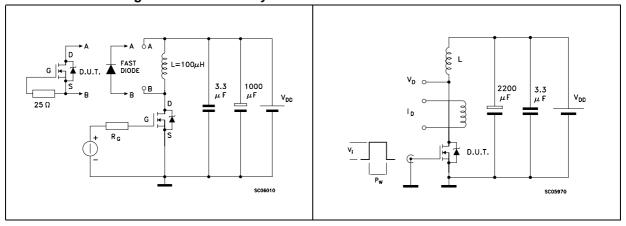
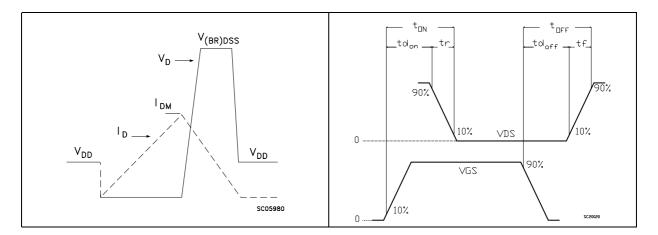


Figure 16. Unclamped inductive waveform

Figure 17. Switching time waveform



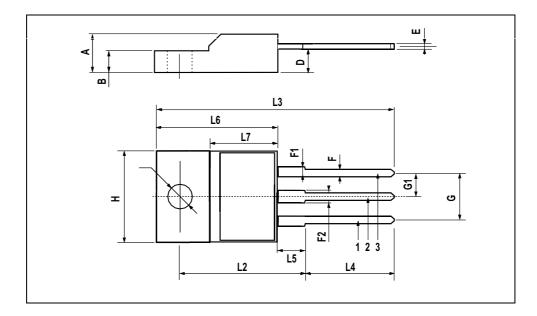
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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TO-220FP MECHANICAL DATA

DIM.		mm.			inch	
DIIVI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX
Α	4.4		4.6	0.173		0.181
В	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
Е	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
Н	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



STP80NF10FP Revision history

5 Revision history

Table 7. Revision history

Date	Revision	Changes
11-Apr-2006	1	First Release

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